# COURSE DESCRIPTION CARD - SYLLABUS

Course name
Design of systems with FPGA [S2EiT2E-TIT>PSzFPGA]

## Course

Field of study
Electronics and Telecommunications

Year/Semester
2/4

Area of study (specialization)
Information and Communication Technologies

Profile of study
general academic

Level of study
second-cycle

Course offered in
English

Form of study
full-time

Requirements
elective

## Number of hours

Lecture
15

Laboratory classes
30

Other
0

Tutorials
0

Projects/seminars
0

## Number of credit points

4,00

## Coordinators

dr hab. inż. Olgierd Stankiewicz prof. PP
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## Lecturers

## Prerequisites

Has basic knowledge of development trends in programmable systems. Has sufficient knowledge to design specialized digital circuits for use in programmable systems. Knows how basic communication interfaces work. Knows the principles of designing basic elements of digital systems (state machines, pipelines). Has general knowledge of information theory. Is able to obtain data from literature and other sources, can integrate obtained information, interpret it, and formulate and justify opinions. Can describe elements of a digital system in the form of Verilog language module. Can test and verify the correct functioning of a digital system. Can use learned design techniques to design a digital system. Can use modern tools to support the design and synthesis of digital systems for the FPGA platform. Is open to learning opportunities and understands the need to improve professional competence. Has basic knowledge necessary to understand non-technical conditions of engineering activities; knows the basic principles of occupational health and safety. Has a sense of responsibility for designed electronic and telecommunication systems.

## Course objective

Expanding the knowledge of programmable FPGA chips, familiarizing with hybrid programmable chips (e.g. ARM processor + FPGA). Getting to know the construction and design methods of SoC (System-on- Chip) systems. Expanding the knowledge of Verilog language and introducing to SystemVerilog: advanced methods of simulation, compilation and synthesis of systems, sample realizations of selected algorithms. Implementation of projects on Xilinx/Lattice FPGA systems.

## Course-related learning outcomes

Knowledge:
Has basic knowledge about hybrid programmable systems.
Has knowledge about the construction and design of SoC systems for FPGA systems.
Knows how fast communication interfaces work.

Skills:
Can obtain data from literature and other sources, he can integrate the information obtained, interpret it, and formulate and justify opinions.
Can describe a complex digital system in the form of a hierarchy of Verilog language modules.
Can correctly define the interface parameters between two frequency domains.

Social competences:
Is open to continuous learning and understands the need to improve professional competence.
Has the basic knowledge necessary to understand non-technical conditions of engineering activities; knows the basic principles of occupational health and safety.
Has a sense of responsibility for designed electronic and telecommunication systems.

## Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

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Lecture: written exam
The written exam is a set of 6-10 problematic questions, for which desciptory answer is expected.
Each answer is ranked from 0 to 1 points (fractinal points also possible).
The exam is passed if the number of attained points is greater than 50%. More than 50% indicates the knowledge above of satisfactory level.
The course issues of which the questions are prepared, are sent to students by e-mail using the university"s e-mail system.
Laboratories:
Activity during classes, reports from particular activities. Laboratory project realized individually/in small groups.

## Programme content

Developments and trends in FPGA circuits based on the example of the latest FPGA programmable circuits from Xilix/Lattice, Multi-Gigabit Serial I/O.
Hybrid-FPGA programmable systems.
Frequency domains - the problem of data transfer between domains, industrial recommendations, circuit synchronization, source-synchronous interface.
Fast I/O interfaces - use of Gigabit GTP, GTX, GTH modules in HD-SDI, SATA, PCI-E, and SerDes.
Systems on Chip (SoC).
Programming languages - Verilog, SystemC, SystemVerilog, migen, MyHDL. Principles of good programming, self-describing listing.
Methods and tools for simulation and synthesis of projects on FPGA chipsets - EDIF file generation, project partitioning, Python scripting language.
Examples of effective implementation of selected algorithms (DCT conversion, RGB>YUV colour space conversion, elementing, composite multiplication, floating point operations), for FPGA systems.

## Course topics

none

## Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.
Laboratories: implementation of projects on computers (individual or in groups of few people).
Examples illustrated on screen/blackboard.

## Bibliography

Basic
Węgrzyn M., Barkalov A., Design of Control Units with Programmable Logic. Zielona Góra 2006.
Skahill K., Język VHDL, WNT, Warszawa 2001.
Additional
Woods R. McAllister J., Yi Y. Lightbody G. FPGA-based Implementation of Signal Processing Systems,Wiley,2008.
Palnitkar S., Verilog HDL (2nd Edition), Prentice Hall Professional, 2003.
Kilts S., Advanced FPGA DESIGN, Wiley 2007.

## Breakdown of average student's workload

| | Hours | ECTS |
|---|---|---|
| Total workload | 100 | 4,00 |
| Classes requiring direct contact with the teacher | 55 | 2,00 |
| Student's own work (literature studies, preparation for laboratory classes/ tutorials, preparation for tests/exam, project preparation) | 45 | 2,00 |